Novel Ruggedized Packaging Technology for VCSELs

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Abstract: *We describe chip-scale packaging (CSP) technology for compact, low-cost optical transceivers that contain OTDR technology. CSP creates board-level solder interconnect at the wafer level, eliminating the cost and parasitics associated with packages. OTDR technology enables insitu monitoring of fiber links.*

Keywords: fiber optics; fiber optic transceivers; vertical cavity surface emitting laser (VCSEL); harsh environment optical interconnects; chip-scale-packaging.

Introduction: Chip-Scale-Packaging for Photonics

Wafer scale processing of metal interconnect [1]-[2] and optical micro-lenses [3]-[4] are becoming mature technologies that address the need for low cost packaging of electronics and optical components. We describe the use of these wafer scale processes to create micro-scale CSP optical transmitters (µTX) and receivers (µRX), (or µTRX collectively). µTRXs are low-cost, compact components that can be assembled onto the PCB in close proximity to high-performance ASICs using conventional solder-reflow 'pick-and-place' assembly. The small PCB footprint and solderability is necessary to achieve high-density and flexible placement of optical components near the data source/sink. By reducing the routing lengths of high-speed copper wiring, we can achieve low-power, EMI-immune links within high-performance military computing and sensor systems.

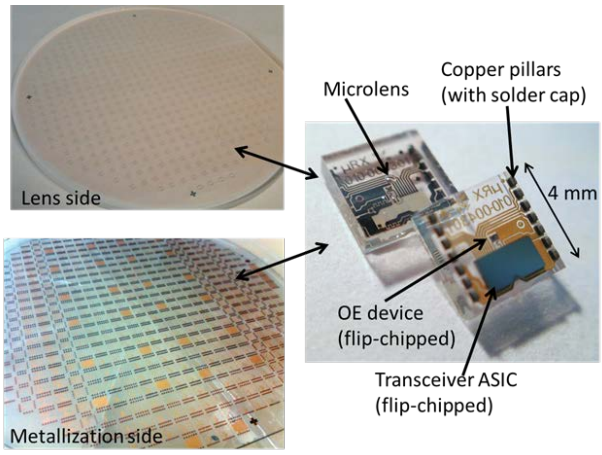

Figure 1. Chip-scale-packaging of micro-transceiver components.

Figure 1 shows an example of a µTRX assembly. Microlens are formed with gray-scale etching on a glass wafer. The reverse-side of this wafer contains three types of metallization: 1) flip-chip bond pads for attachment of OE devices (such as VCSELs and PINs) and ASICS (such as a VCSEL driver or receiver), 2) routing of signals, and 3) copper pillars with solder caps for soldering to a PCB. The lenses and reverse-side metallization are aligned at the wafer level to sub-micron tolerances, allowing the passive alignment of the OE device to the lens with flip-chip bonding. The resulting optical component has a PCB footprint of (4 x 4 mm2). This package has no wire-bonds and has minimum electrical parasitics, and is therefore minimizes the EMI and scales to future data rates.

Integration of OTDR ASICs within EOM

The availability of high-speed ASIC technology makes it possible to integrate the functions required to create OTDR measurements on a single chip. Figure 2 shows the OTDR ASIC, code named "NAVCAT", which is the single chip integration of programmable timing circuits that operate up to 10 GHz, a pattern generator (arbitrary 20-bit pattern) output in a CML signal format, and a four-channel receiver/sampling circuit. The NAVCAT can generate pulse widths of 100 ps and sample at 100 ps resolution. Note: the round-trip time for an optical pulse to travel 1 cm in fiber is 100 ps.

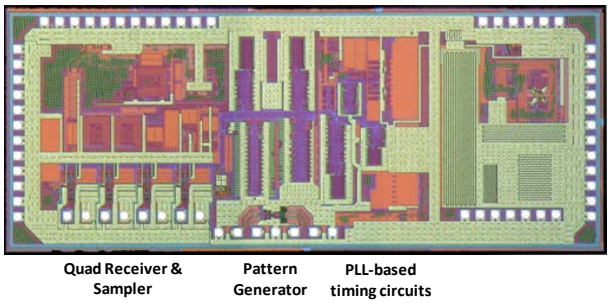

Figure 2: OTDR ASIC "NAVCAT"

In OTDR operation, the NAVCAT generates a pulse on the CML output and samples a receiver channel at an instance corresponding to the distance along the fiber under measurement. The NAVCAT receivers are dual-sampling, which can make pre/post pulse measurements for noise cancelation. The samples are digitized, averaged to increase the signal-to-noise ratio (SNR), and then available for read-out on a digital bus. NAVCAT has four receiver channels. When combined with a quad transceiver ASIC capable of

10 Gbps (i.e., compatible with a 100 ps bit period), the chipset can perform OTDR measurements on the transmit fibers within a quad transceiver module.

The NAVCAT is agnostic to the optical wavelength or fiber type. Figure 3 shows the general OTDR block diagram. The blue blocks are elements normally found within a non-BIT OTDR capable transceiver. The NAVCAT OTDR function is inserted into the data path with a mux, and the back-reflected light is split into an additional detector (such as a receiver optical subassembly

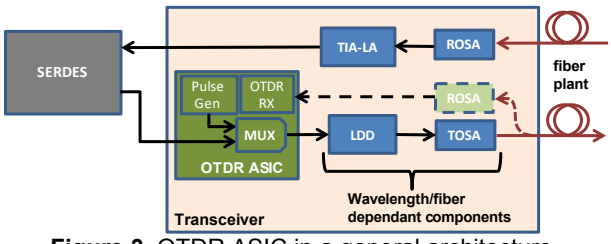

Figure 3. OTDR ASIC in a general architecture.

(ROSA)).

Successful transition of OTDR functionality into EOM transceivers will require packaging compatible with compact assemblies. We present a method of incorporating the OTDR ASIC chipset into a low-form-factor quad transceiver with data rates of 10 Mbps to 12.5 Gbps per channel. The rugged vertical connector (RVCON™) provides a collimated optical beam interface to a "CORE" sub-assembly containing transceiver ASICs, optoelectronic components and sealed collimating lenses. The cross-section shows the packaging of the OTDR chipset, VCSEL, PIN photodiode, and OTDR splitting optics.

Test Results of Quad Transceiver

The technology was used to create a 4-channel Tx and 4-channel Rx fiber optic transceiver (XCVR) with microcontroller that operates from data rates of 10 Mbps to 12.5 Gbps per channel (see Figure 4). The XCVR is based on a CSP that contains all active elements and the optical coupling system.

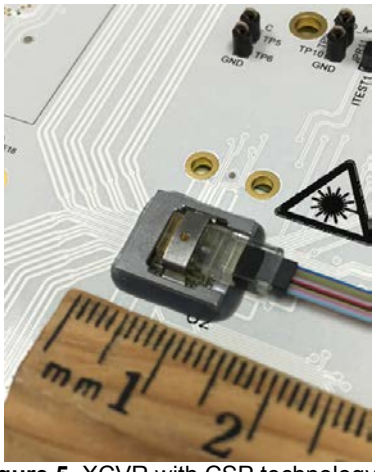

Figure 5. XCVR with CSP technology.

The XCVR meets the specifications for 10 Gigabit Ethernet (10GBASE-SR) over the temperature range of -40 C to 95 C. Figure 2 and Figure 3 show the results of 10GBASE-SR compliance testing at 10.3125 Gbps data rate. The receiver eye diagrams are measured with an optical input power of -11.1 dBm optical modulation amplitude (OMA). The typical sensitivity of the X80-QC at 10.3125 is -12.6 dBm OMA.

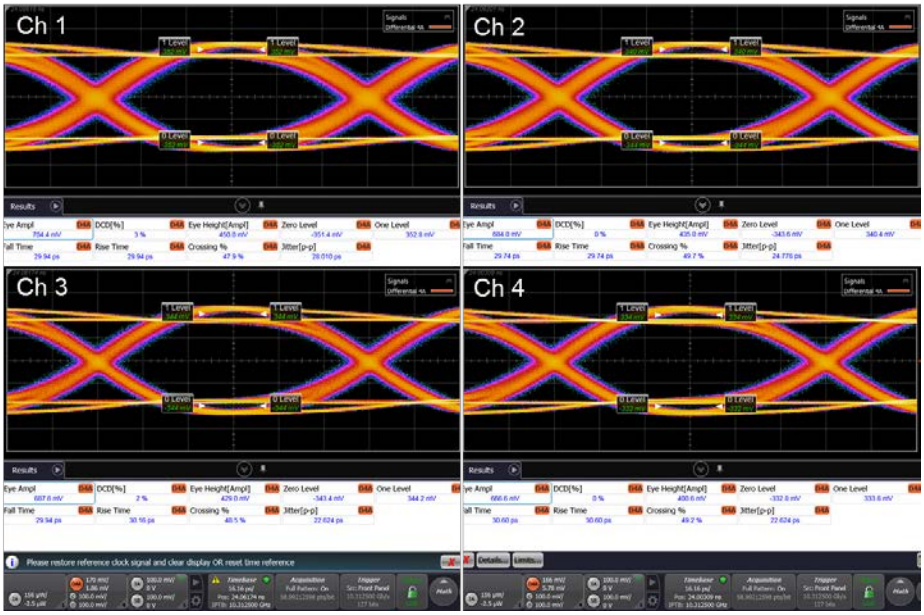

Figure 4. 10GBASE-SR compliance testing on receiver channels with -11.1 dBm (OMA) input.

The transmitter testing against the 10G BASE-SR mask shows a minimum 40% mask margin. The transmitter average optical power was -2.5 dB m in these measurements. The VCSEL output is attenuated with a 4 dB attenuation coating patterned in the optical path (on the transmit side only). To achieve increase optical power output, this attenuation can be reduced.

Conclusion

CSP technology enables low-cost, embedded transceivers for short length communications. As fiber becomes more prevalent for short distance links, fiber networks can have a number of short span links (chip-chip, board-to-board, etc). In large scaled deployment, the fiber system may be vulnerable to fiber faults, especially at the connection interfaces. To address the cost associated with fiber system maintenance and to enhance overall network availability, ARMY initiated programs to develop built-in-test (BIT) within the transceiver components. BIT capability can detect and isolate the faults within the transceiver and along the fiber path allowing for quick and accurate resolution.

Acknowledgements

This work was performed under the following SBIR contracts: Army Research Lab: Michael Gerhold (TPOC), Dept of Energy: Rich Carlson (TPOC), and NAVAIR: Mark Beranek (TPOC)

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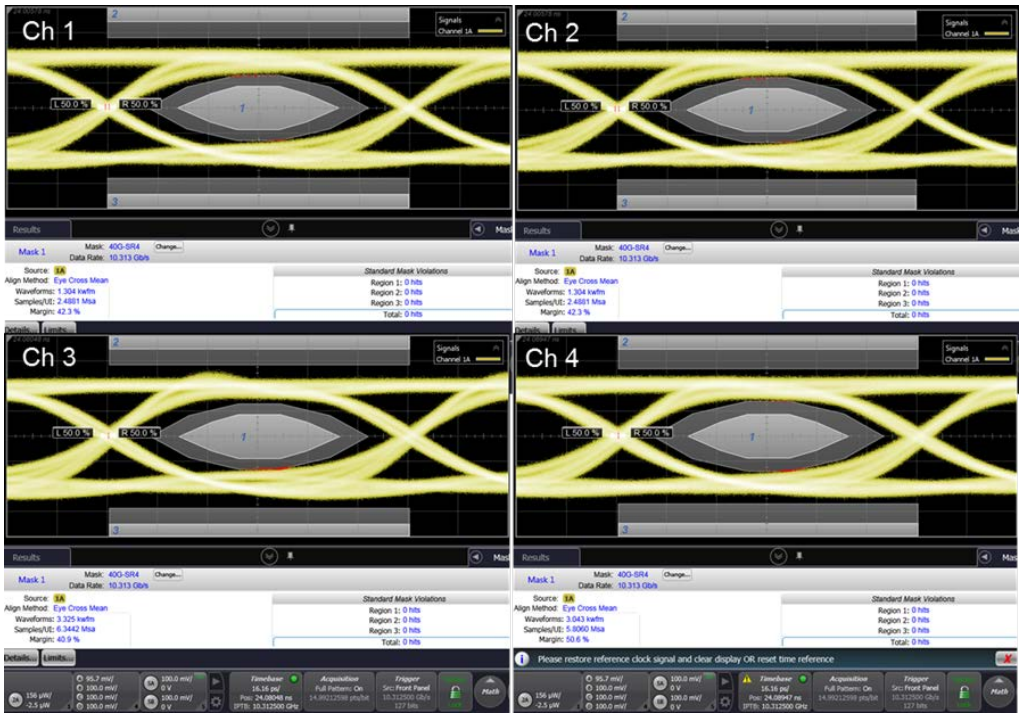

Figure 6. 10GBASE-SR compliance testing on transmitter channels.